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Program : **B.Tech**

Subject Name: **Computer System Organisation**

Subject Code: **EC-504**

Semester: **5th**

# Unit V

## Multiprocessors

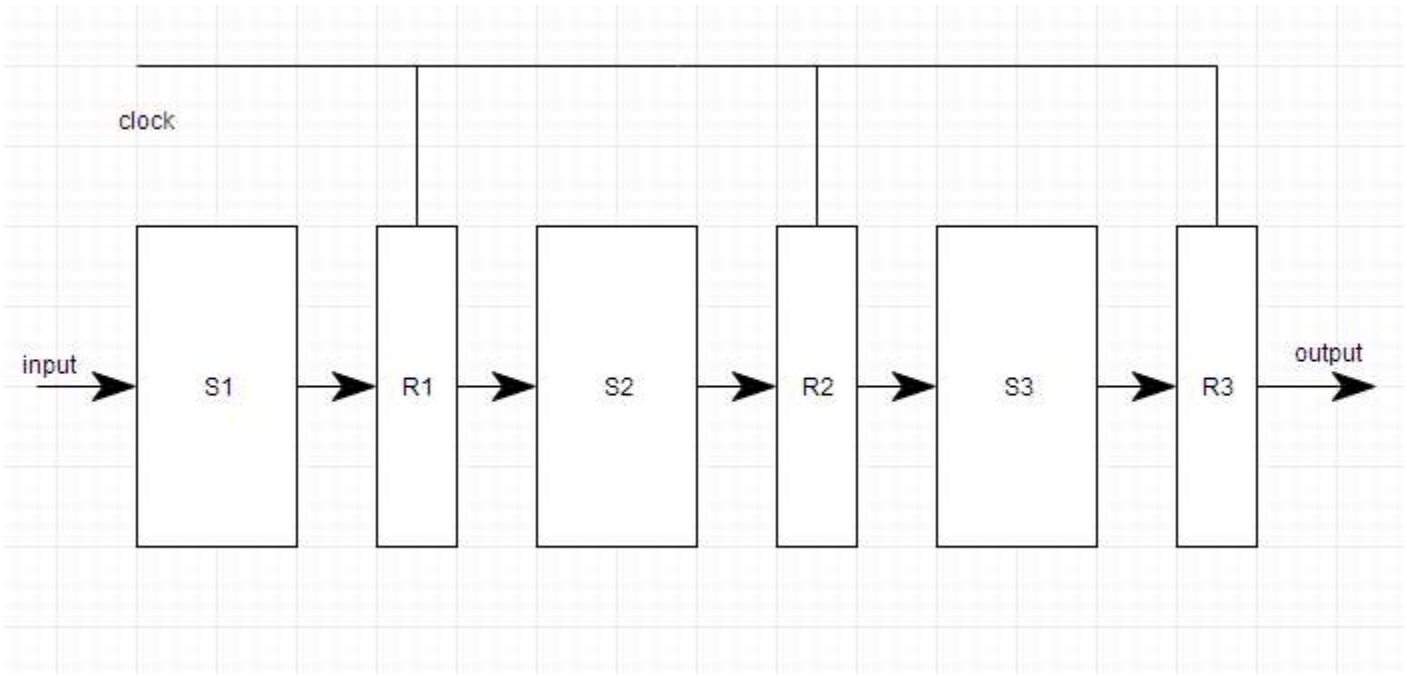
### 5.1 Pipeline Processing and Types of Pipelines

Pipelining is the process of accumulating instruction from the processor through a pipeline. It allows storing and executing instructions in an orderly process. It is also known as pipeline processing.

Pipelining is a technique where multiple instructions are overlapped during execution. Pipeline is divided into stages and these stages are connected with one another to form a pipe like structure. Instructions enter from one end and exit from another end.

Pipelining increases the overall instruction throughput.

In pipeline system, each segment consists of an input register followed by a combinational circuit. The register is used to hold data and combinational circuit performs operations on it. The output of combinational circuit is applied to the input register of the next segment.




Pipeline system is like the modern day assembly line setup in factories. For example in a car manufacturing industry, huge assembly lines are setup and at each point, there are robotic arms to perform a certain task, and then the car moves on ahead to the next arm.

Types of Pipeline

It is divided into 2 categories:

1. Arithmetic Pipeline
2. Instruction Pipeline

Arithmetic Pipeline

Arithmetic pipelines are usually found in most of the computers. They are used for floating point operations, multiplication of fixed point numbers etc. For example: The input to the Floating Point Adder pipeline is:

$X = A*2^a$

$Y = B*2^b$

Here A and B are mantissas (significant digit of floating point numbers), while a and b are exponents.

The floating point addition and subtraction is done in 4 parts:

1. Compare the exponents.
2. Align the mantissas.
3. Add or subtract mantissas
4. Produce the result.

Registers are used for storing the intermediate results between the above operations.

Instruction Pipeline

In this a stream of instructions can be executed by overlapping *fetch*, *decode* and *execute* phases of an instruction cycle. This type of technique is used to increase the throughput of the computer system.

An instruction pipeline reads instruction from the memory while previous instructions are being executed in other segments of the pipeline. Thus we can execute multiple instructions simultaneously. The pipeline will be more efficient if the instruction cycle is divided into segments of equal duration.

Pipeline Conflicts

There are some factors that cause the pipeline to deviate its normal performance. Some of these factors are given below:

1. Timing Variations

All stages cannot take same amount of time. This problem generally occurs in instruction processing where different instructions have different operand requirements and thus different processing time.

2. Data Hazards

When several instructions are in partial execution, and if they reference same data then the problem arises. We must ensure that next instruction does not attempt to access data before the current instruction, because this will lead to incorrect results.

3. Branching

In order to fetch and execute the next instruction, we must know what that instruction is. If the present instruction is a conditional branch, and its result will lead us to the next instruction, then the next instruction may not be known until the current one is processed.

4. Interrupts

Interrupts set unwanted instruction into the instruction stream. Interrupts effect the execution of instruction.

5. Data Dependency

It arises when an instruction depends upon the result of a previous instruction but this result is not yet available.

Advantages of Pipelining

1. The cycle time of the processor is reduced.
2. It increases the throughput of the system
3. It makes the system reliable.

Disadvantages of Pipelining

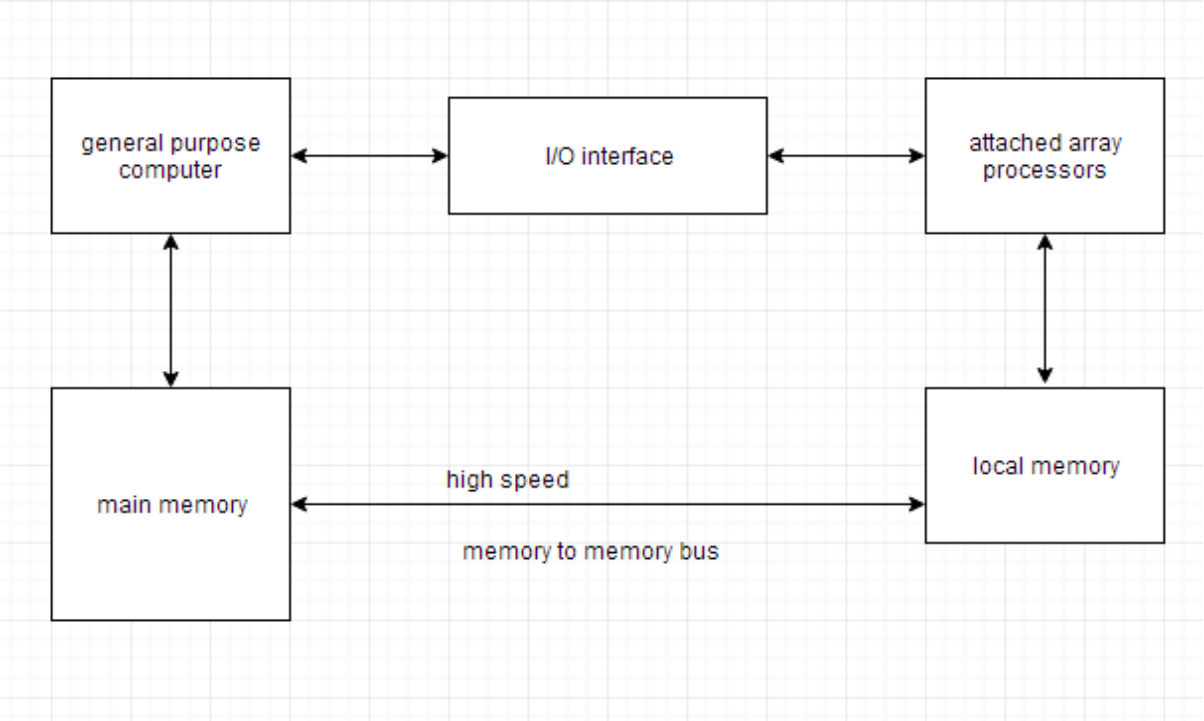
1. The design of pipelined processor is complex and costly to manufacture.
2. The instruction latency is more.

## 5.2 Vector (Array) Processors

A vector processor is a central processing unit that can work on an entire vector in one instruction. The instruction to the processor is in the form of one complete vector instead of its element. Vector processors are used because they reduce the draw and interpret bandwidth

owing to the fact that fewer instructions must be fetched. A vector processor is also known as an array processor.

Vector processors are the technology used in modern computers and central processing units because many performance optimization methodologies are applied in them. To reduce store and load latency, memory banks are utilized and in case of large multimedia applications, data parallelism is being applied. Vector instruction sets are designed over an innovative architecture which saves memory and time for a machine. The high on-chip memory microchips used for vector processing are expensive, so the design cost of such processors is usually very high.



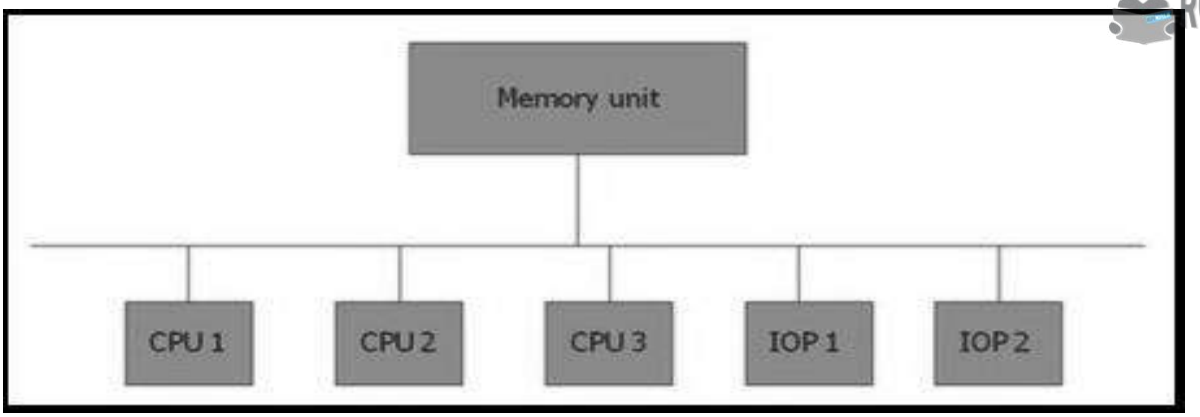

## 5.3 Interconnection Structure

The components that form a multiprocessor system are CPUs, IOPs connected to input-output devices, and a memory unit. The interconnection between the components can have different physical configurations, depending on the number of transfer paths that are available. Between the processors and memory in a shared memory system. Among the processing elements in a loosely coupled system.

There are several physical forms available for establishing an interconnection network.

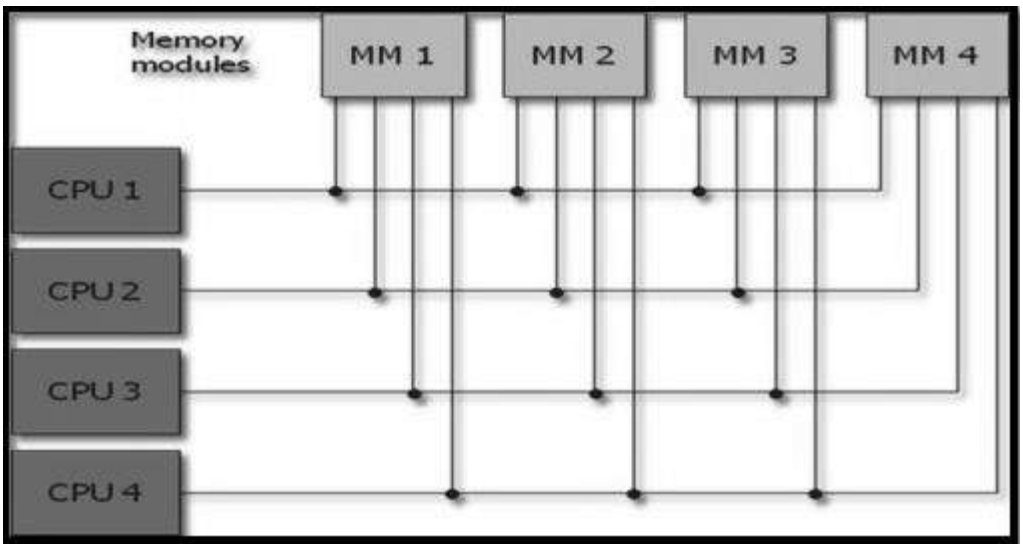
1.Time-shared common bus

Consists of a number of processors connected through a common path to a memory unit. Part of the local memory may be designed as a cache memory attached to the CPU. Only one processor can communicate with the memory or another processor at any given time. The total transfer rate within the system is limited by the speed of the single path.



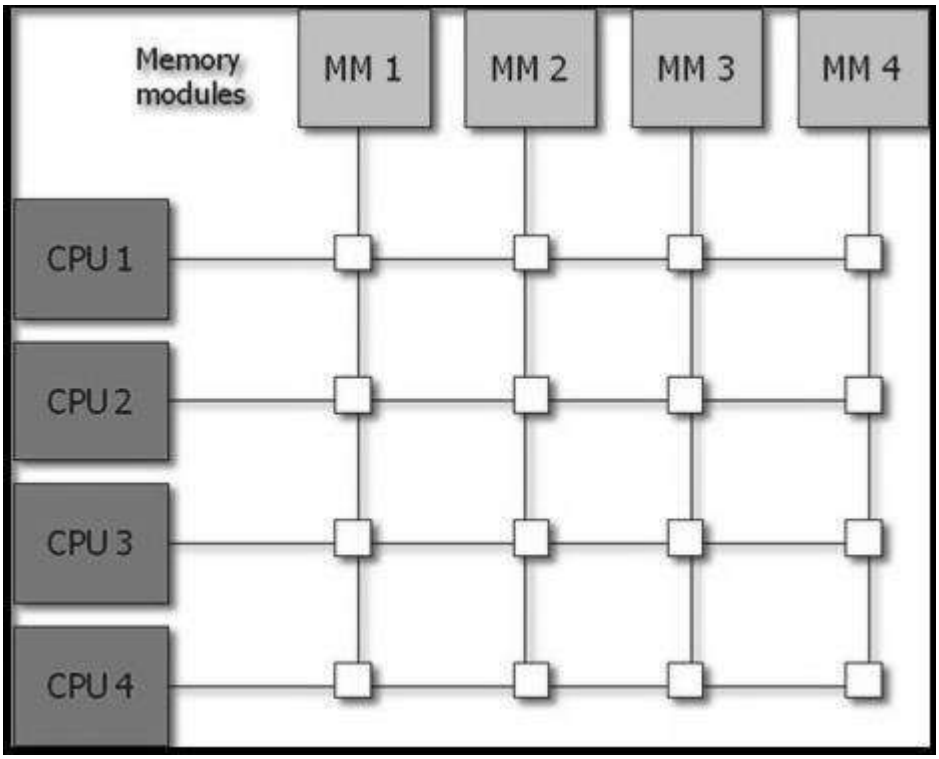

2. Multiport memory

In the multiport memory system, different memory module and CPUs have separate buses. The module has internal control logic to determine port which will access to memory at any given time. Priorities are assigned to each memory port to resolve memory access conflicts. Because of the multiple paths high transfer rate can be achieved .It requires expensive memory control logic and a large number of cables and connections.




3. Crossbar switch

Consists of a various number of cross points that are present at intersections between processor buses and memory module paths. A switch determines the path from a processor to a memory module. Supports simultaneous transfers from all memory modules. The hardware required to implement the switch can be very large and complex.

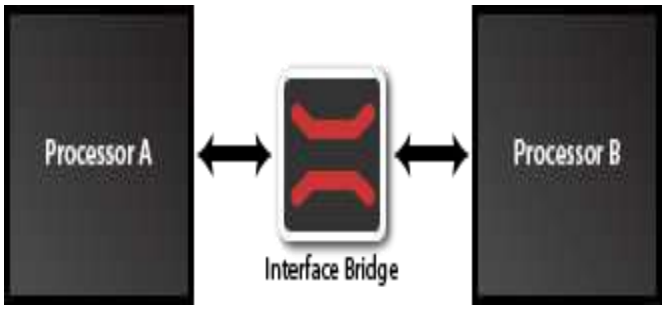



## 5.4 Inter Processor Communication(IPC)

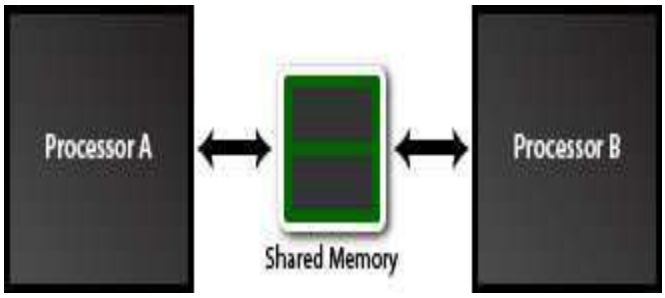
Inter-Processor Communication (IPC) is a set of methods of exchanging data between two processors. These two processors can be any combination of application processors, baseband processors, connectivity processors and/or media processors. The most common examples of IPC use is dual mode phones and data cards. Processors are not designed to talk to each other. Most interfaces found in processors are masters or host controllers, such as I²C master, SPI master, and SDIO host controller. The master and host controller need to connect to a slave or a client controller.

IPC technology provides system designers a quick and easy method to build a common communication scheme between two processors. There are two types of architecture available for the designer to choose from:

1) Direct Communication Scheme( Interface bridge)



2) Indirect Communication Scheme

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